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10/687,827	10/20/2003	Ronald Chi-Chun Hui	20599.0002	9906

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EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 06/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,827	HUI, RONALD CHI-CHUN	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory Primary Examiner 6/8/2006

FRITZ FLEMING

GR. AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

FnF 6/8/2006

1. Claims 3 and 6-7 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 3 and 6-7, it is unclear how each of the corresponding claims are dependent on itself. Examiner will assume that claims 3 and 6-7 are dependent on independent claim 1 for the current examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roskowski et al. (US Patent 5,257,385) in view of Hegde (US Patent 6,570,875).

As per claim 1, Roskowski teaches a memory switched switching apparatus comprising:

a memory queue (Fig. 1, ref. 16) for storing queuing elements (col. 4, ll. 21-23);

rowmin logic (Fig. 2, ref. 25) coupled to the memory for determining the highest priority queuing element for each row (col. 5, ll. 1-13 and col. 5, ll. 36-43);

global min logic (Fig. 1, ref. 27, 34) coupled to the rowmin logic for identifying the highest priority queuing element for each port (col. 7, ll. 58-62); and

a scheduler (control circuit 17 of Fig. 1) coupled to the global min logic, the scheduler dequeuing the packets for each port by outputting the packet associated with the highest priority queuing element for each port identified by the global min logic (col. 8, ll. 1-4).

Roskowski does not expressly teach the memory switched switching apparatus comprising wherein the memory having addresses that identify the flow_id of individual flows.

Hegde teaches a system and a method for packet switching comprising:

a multiprotocol switch (Fig. 2, ref. 40) including a switch module (Fig. 2, ref. 60) and a flow table (Fig. 2, ref. 70), wherein when a packet is received the packet's header information including the address of the communication hosts (source and destination) are extracted for the purpose of performing flow identification utilizing the flow table (col. 5, ll. 40-49 and col. 7, ll. 5-15).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hegde's header information into Roskowski's memory

switching apparatus. The resulting combination of the references teaches the memory switch further comprising the extraction of the addresses from the buffered packets for the purpose of flow identification.

Therefore, it would have been obvious to combine Hegde with Roskowski for the benefit of reduce administrative overhead and automatic maintaining forwarding information without any administrative intervention (Hegde, col. 2, ll. 1-15).

3. As per claim 2, Roskowski and Hegde teach all the limitation of claim 1 as discussed above, where Hegde further teaches the memory switched switching apparatus comprising wherein each row stores queuing elements for more than one output port (Hegde, col. 1, ll. 58-62), as the packet is forwarded by broadcasting and multicasting, the packet is forwarded to more than one output port.

4. As per claim 3, Roskowski and Hegde teach all the limitation of claim 1 as discussed above, where Hegde further teaches the memory switched switching apparatus comprising wherein the row min logic includes a filtering element for excluding from the highest priority level determination for each port within each row the priority level of queuing elements associated with other ports (Hegde, col. 6, ll. 5-13), wherein a filter is utilized to forbid communication between two ports, therefore the filter may be utilized for excluding from the highest priority level determination for each port within each row the priority level of queuing elements associated with other ports as there may be restriction associated with the communication.

5. As per claim 4, Roskowski and Hegde teach all the limitation of claim 1 as discussed above, where Hegde further teaches the memory switched switching apparatus comprising wherein each row stores queuing elements for only one output port (Hegde, col. 24, ll. 28-32), as the packet is forwarded by unicasting, the packet is forwarded to only one output port.

6. As per claim 6, Roskowski and Hegde teach all the limitation of claim 1 as discussed above, where Hegde further teaches the memory switched switching apparatus comprising wherein each queuing element includes a valid flag which is set to valid when the queuing element stores a priority level of a packet in the queue and set to invalid after the queuing element is dequeued (Hegde, col. 8, ll. 43-49), wherein the setting of the flag is utilized for configuring the enabling or disabling of a function, therefore it would be obvious to utilized the flag for configuring the validation (enabling) of the function for the queuing element associated with the setting of the packet's priority level.

7. As per claim 7, Roskowski and Hegde teach all the limitation of claim 1 as discussed above, where Roskowski further teaches the memory switched switching apparatus comprising wherein the dequeued queuing element is replaced by the queuing element corresponding to the next packet in the flow after a dequeue operation (Roskowski, Fig. 1, ref. 16 and col. 4, ll. 21-27), as each of the buffer memory is

associated with a specific port to a specific component, therefore when the buffered element is dequeued (outputted), the following packet to replace the just emptied buffer space would be from the same specific port from the same specific component of the just dequeued element, therefore from the same flow.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roskowski et al. (US Patent 5,257,385) and Hegde (US Patent 6,570,875), and further in view of Wicklund (US Patent 6,295,295).

Roskowski and Hegde teach all the limitation of claim 1 as discussed above.

Roskowski and Hegde does not teach the memory switched switching apparatus comprising wherein each queuing element includes a pointer to a linked list of other queuing elements for the flow.

Wicklund teaches a scheduler for an information packet switch comprising a current queue (Fig. 4, ref. 42) having a pointer pointing to a link list of data to be transferred (Fig. 4 and col. 6, ll. 56-64), wherein the link list is established as each of the blocks of data have a pointer pointing to the next block of data to be transferred, thus forming a single logical link.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Wicklund's pointer to the link list of data blocks into Roskowski and Hegde's queuing element. The resulting combination of the references teaches the memory switched switching apparatus further comprising the queuing

element having the pointer pointing to the link list of packets, therefore forming the single logical link comprising packets from the same flow.

Therefore, it would have been obvious to combine Wicklund with Roskowski and Hegde for the benefit of providing the globally fair control of sharing of the available bandwidth in the packet switch (Wicklund, col. 4, ll. 8-16).

9. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hegde (US Patent 6,570,875) in view of Li et al. (US Patent 6,560,230).

10. As per claim 8, Hegde teaches a method of scheduling packets within a memory switched architecture, comprising:

maintaining a shared priority queue (Fig. 4, ref. 120) having queuing elements associated with multiple flows and multiple output ports (Fig. 2, ref. 50 and col. 1, ll. 58-62), wherein multiple flow of packets are received and broadcasted (multicasted) therefore the packets are forwarded to multiple output ports;

determining a priority level for a newly arriving packet based on its flow identification (Fig. 8, ref. S44, S46; Fig. 12, ref. S170, S172 and col. 7, ll. 5-15), wherein upon implementing flow identification, the priority level associated with identified flow is determined and a priority level of a queuing entry in the priority queue corresponding to the flow identification (Fig. 12, ref. S172, S176 and col. 16, ll. 34-38), wherein the determination of the flow's priority results in determining of which of the eight I/O

queues (priority queue) the flow's packet would be forwarded, as each I/O queue have the corresponding priority level associated with the priority level of the packet; and

storing a new queuing element corresponding to the newly arriving packet in the priority queue based on its flow identification (Fig. 12, ref. S176)

Hegde does not teach the method of scheduling packets within a memory switched architecture, comprising wherein the new queuing element including its determined priority level.

Li teaches a packet scheduling method and apparatus comprising the buffering of packets in a plurality of buffers (Fig. 5, ref. 64), wherein the data fields of the buffered packed includes the type of service (Fig. 3) (col. 8, ll. 34-37), as it is well known that the type of service data field provides the priority level associated with the buffered packet.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hegde's priority data field into Li's new queue element.

Therefore, it would have been obvious to combine Hegde with Li as the packet to be transferring includes the priority data field is well known in the art, and further more, providing the benefit of fair scheduling in the transferring of real-time packets (higher priority packets) and non-real time packets (lower priority packets) (Hegde, col. 3, ll. 50-53).

11. As per claim 9, Hegde and Li teach all the limitation of claim 8 as discussed above, where Li further teaches the method of scheduling packets within a memory switched architecture, comprising wherein the shared priority queue includes rows

comprising multiple columns for storing multiple queuing elements (Li, Fig. 5, ref. 64), wherein each row of buffer queues the plurality of packets, therefore forming the columns, such as the first column includes all the first packets that are to be outputted for each row.

12. As per claim 10, Hegde and Li teach all the limitation of claim 9 as discussed above, where both further teaches the method of scheduling packets within a memory switched architecture, comprising wherein each queuing element stores an output port identifier (Li, destination address of Fig. 3) specifying an output port for its corresponding packet (Li, Fig. 3 and Hegde, Fig. 4, ref. 120), as the destination address provide information associated with where the packet is to be routed therefore specifying which port the packet would be queued and then transferred.

13. Claims 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hegde (US Patent 6,570,875) and Li et al. (US Patent 6,560,230), and further in view of Roskowski et al. (US Patent 5,257,385).

14. As per claim 11, Hegde and Li teach all the limitation of claim 10 as discussed above.

Hegde and Li does not expressly teach the method of scheduling packets within a memory switched architecture, further comprising determining whether the new queuing element has the highest level of priority for the same output port.

Roskowski teaches a system and a method comprising determining the highest level of priority for the single output node (Fig. 2; col. 5, ll. 59-62 and col. 7, ll. 58-62) wherein the determination is implemented continuously, therefore whenever there is a newly buffered data to be transferred, the determination if the newly buffered data has the highest level priority level would be implemented.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Roskowski's determining the data with the highest priority into Hegde and Li's scheduling of packets.

Therefore, it would have been obvious to combine Roskowski with Hegde and Li for the benefit of proper arbitration of data to be transferred (Roskowski, col. 2, ll. 26-41).

15. As per claim 12, Hegde, Li and Roskowski teach all the limitation of claim 11 as discussed above, where Roskowski further teaches the method of scheduling packets within a memory switched architecture, further comprising updating a rowmin value (Roskowski, highest priority value associated with each node outputted by the comparator circuit 25 of Fig. 2) when the new queuing element has the highest level of priority for the same output port on a row (Roskowski, Fig. 2), wherein each of the comparator circuit compares the row of packets associated with the corresponding node A, node B and node C, and outputs the updated highest priority value (rowmin value).

16. As per claim 13, Hegde, Li and Roskowski teach all the limitation of claim 12 as discussed above, where Roskowski further teaches the method of scheduling packets within a memory switched architecture, further comprising determining whether the new queuing element has the highest level of priority among all of the queuing elements in the priority queue for the same output port (Roskowski, Fig. 2 and col. 7, ll. 58-62).

17. As per claim 14, Hegde, Li and Roskowski teach all the limitation of claim 13 as discussed above, where Roskowski further teaches the method of scheduling packets within a memory switched architecture, further comprising updating a globalmin value (Roskowski, the signal output by the comparator circuit 34 of Fig. 2) when the new queuing element has the highest level of priority for the same output port within the priority queue (Roskowski, Fig. 2 and col. 7, ll. 58-62), as the signal (globalmin value) output by the comparator circuit (Roskowski, Fig. 2, ref. 34) provides the choice selecting the buffered packet with the highest level of priority among all buffered packets.

18. As per claim 15, Hegde, Li and Roskowski teach all the limitation of claim 14 as discussed above, where all further teach the method of scheduling packets within a memory switched architecture, further comprising selecting an output port (Hegde, Fig. 12, ref. S154, wherein the port(s) associated with the packet's destination is determined) for dequeuing and outputting to the switching matrix the flow identifier and priority level corresponding to the global min value for the selected port (Hegde, Fig. 2

and col. 5, ll. 39-43; Li, Fig. 3 and Roskowski, Fig. 2), wherein upon receiving the packet, said packet includes necessary information in the header for flow identification (Hegde, col. 5, ll. 39-43) and the priority level (Li, Fig. 3) would be forwarded (outputted) to the to the switch module (Hegde, Fig. 2, ref. 60) base on determining which of the received buffered packet have the highest priority (Roskowski, Fig. 2).

19. As per claim 16, Hegde, Li and Roskowski teach all the limitation of claim 15 as discussed above, where all further teach the method of scheduling packets within a memory switched architecture, further comprising outputting a packet from the selected output port based on the flow identifier corresponding to the global min value for the selected port (Hegde, Fig. 12, ref. S176 and Roskowski, Fig. 2), wherein the packet is forwarded to be outputted through the determined port, base on determining which of the received buffered packet have the highest priority.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C.K.L.
06/06/2006

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6/8/2006